IN THE SPECIFICATION:

Please amend the paragraph beginning on page 19 at line 16 as follows:

--As described above, the power supply voltage VddC changes in pulse form. Here, the high-level potential and low-level potential of the power supply voltage VddC are noted as VddC_H and VddC_L, respectively (see FIG. 4B). The actual value of VddC_H is 2.8 V, for example. A voltage which varies within a range from 0 V to 2.8 V is applied to the gates of the reset transistors 5; the channel potentials obtained when a low-level potential (0 V) is applied to the gates of the reset transistors 5 are noted as ~~TRchL~~ RSchL. A voltage which varies in a range from 0 V to 2.8 V is also applied to the gates of the transfer gates 2; the channel potentials obtained when a low-level potential (0 V) is applied to the gates of the transfer gates 2 are noted as TRchL. With the use of the notation, in the present embodiment, the low-level potential VddC_L of the power supply voltage is controlled such that the following relationship(s) holds:

RSchL < VddC_L ... (1) and/or

TRchL < VddC_L ... (2).--